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number with the Hex to **temperature conversion table**. ... routine is a **table lookup**, which picks up a number. from PE0 and compares ...

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converter gives **temperature** in digital form. These data are. used by the microcomputer to generate the varactor voltage. using a small **look-up table** and ...

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lookup table and is. presented serially. **Temperature conversion** accuracy. is *OS°C from 0°C to 70°C (32°F to. 158°F). The error increases to *l°C ...

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The DS1920 can measure **temperature** over the range of -55°C to +100°C in 0.5°C increments. For Fahrenheit usage, a **lookup table** or **conversion** factor must be ...

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For Fahrenheit usage, a **lookup table**. or **conversion** factor must be used. Since data is transmitted over the 3-wire bus LSB first, **temperature** data can be ...

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temperature conversions, the **conversion** charge from the **lookup table** is multiplied by 8.

The charge for a humidity. **conversion** is a **temperature**-independent ...

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Each **look-up table** contains 72 bytes (00 to 47h): location 00 corresponds ... offset vary with **temperature**. G1 describes the **conversion** in Equation 2; the ...

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is used to **convert** the digital values into **temperature** and display them on an LCD. ...

couple ADC value and a **look-up table**. After the **temperature** is ...

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describes the RTD PT100 **temperature** transducer, and explains a simple ... A **lookup table** located in μ P memory allows an application to **convert** (through ...

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Temperature Sensor with **Look Up Table** Memory and DAC. FEATURES ... both the A/D **converter** and **look-up. tables**, and directly setting the D/A **converter** input ...

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L2	142	(chambers.in. and peter.in.) or (judkins.in. and josheph.in.)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/01/15 15:34
L3	15	2 and conversion	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/01/15 15:41
L4	931	708/200-206.ccls. and @ad<"20031215"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/01/15 15:49
L5	484	4 and (LUT\$1 or table\$1)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/01/15 16:08
L6	149	(index or indecis) and 5	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/01/15 15:43
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L8	37	708/206.ccls. and @ad<"20031215"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/01/15 15:53

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Chambers, P.; Rockwood, A.;
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Volume 15, Issue 5, Sept. 1995 Page(s):7 - 11
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- ☐ **4. Fibre optic LED-based correlation spectroscopy for O/sub 2/ detection**
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
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- ☐ 4. **Broad-band erbium-doped fiber amplifier flattened beyond 40 nm using long-period grating filter**
Wysocki, P.F.; Judkins, J.B.; Espindola, R.P.; Andrejco, M.; Vengsarkar, A.M.;
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Ronan, M.T.; Lee, K.L.; Corredoura, P.; Judkins, J.G.;
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14. Intelligent thermal management using brushless DC fans-implementing reliable, full-featured, and cost-effective systems for cooling and thermal supervision
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JUDKINS, JOSEPH JAMES III	AUSTIN	TEXAS

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Application#	Patent#	Status	Date Filed	Title	Inventor Name
<u>08542856</u>	<u>5825834</u>	250	10/13/1995	FAST RESPONSE SYSTEM IMPLEMENTING A SAMPLING CLOCK FOR EXTRACTING STABLE CLOCK INFORMATION FROM A SERIAL DATA STREAM WITH DEFINE JITTER CHARACTERISTICS AND METHOD THEREFOR	CHAMBERS, PETER
<u>08578120</u>	<u>5764642</u>	150	12/26/1995	A SYSTEM FOR COMBINING DATA PACKETS FROM MULTIPLE SERIAL DATA STREAMS TO PROVIDE A SINGLE SERIAL DATA OUTPUT AND METHOD THEREFOR	CHAMBERS, PETER
<u>08627986</u>	<u>5774744</u>	150	04/08/1996	A SYSTEM USING DMA AND DESCRIPTOR FOR IMPLEMENTING PERIPHERAL DEVICE BUS MASTERING VIA A UNIVERSAL SERIAL BUS CONTROLLER OR AN INFRARED DATA ASSOCIATION CONTROLLER	CHAMBERS, PETER
<u>08627987</u>	<u>5774743</u>	250	04/08/1996	SYSTEM FOR IMPLEMENTING PERIPHERAL DEVICE BUS MASTERING IN MOBILE COMPUTER VIA MICRO-CONTROLLER FOR PROGRAMMING DMA CONTROLLER, GENERATING AND SENDING COMMAND SIGNALS, AND RECEIVING COMPLETION STATUS	CHAMBERS, PETER
<u>08627988</u>	<u>5809333</u>	250	04/08/1996	SYSTEM FOR IMPLEMENTING PERIPHERAL DEVICE BUS MASTERING IN DESKTOP PC VIA HARDWARE STATE MACHINE FOR PROGRAMMING DMA CONTROLLER, GENERATING COMMAND SIGNALS AND RECEIVING COMPLETION STATUS	CHAMBERS, PETER
<u>08627989</u>	<u>5905912</u>	150	04/08/1996	SYSTEM FOR IMPLEMENTING PERIPHERAL DEVICE BUS MASTERING IN A COMPUTER USING A LIST PROCESSOR FOR ASSERTING AND RECEIVING CONTROL SIGNALS	CHAMBERS, PETER

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<u>08627992</u>	<u>5845151</u>	150	04/08/1996	A SYSTEM USING DESCRIPTOR AND HAVING HARDWARE STATE MACHINE COUPLED TO DMA FOR IMPLEMENTING PERIPHERAL DEVICE BUS MASTERING VIA USB CONTROLLER OR IRDA CONTROLLER	CHAMBERS, PETER
<u>08629015</u>	<u>5933609</u>	150	04/08/1996	METHOD AND SYSTEM FOR HOT DOCKING A PORTABLE COMPUTER TO A DOCKING STATION VIA THE PRIMARY PCI BUS	CHAMBERS, PETER
<u>08703712</u>	<u>5845096</u>	250	08/26/1996	ADAPTIVE ARBITRATION MECHANISM FOR A SHARED MULTI-MASTER BUS	CHAMBERS, PETER
<u>08712089</u>	<u>5845130</u>	250	09/11/1996	MAILBOX TRAFFIC CONTROLLER	CHAMBERS, PETER
<u>08717529</u>	<u>5987584</u>	150	09/17/1996	WAVETABLE ADDRESS CACHE TO REDUCE ACCESSES OVER A PCI BUS	CHAMBERS, PETER
<u>08718086</u>	<u>5933610</u>	250	09/17/1996	PREDICTIVE ARBITRATION SYSTEM FOR PCI BUS AGENTS	CHAMBERS, PETER
<u>08740501</u>	<u>5870570</u>	150	10/29/1996	MULTIPLE BUS AGENT INTEGRATED CIRCUIT DEVICE FOR CONNECTING TO AN EXTERNAL BUS	CHAMBERS, PETER
<u>08754961</u>	<u>6047365</u>	150	11/22/1996	MULTIPLE ENTRY WAVETABLE ADDRESS CACHE TO REDUCE ACCESSES OVER A PCI BUS	CHAMBERS, PETER
<u>08760701</u>	<u>5915103</u>	150	12/05/1996	METHOD AND SYSTEM FOR AN EXTENSIBLE ON SILICON BUS SUPPORTING MULTIPLE FUNCTIONAL BLOCKS	CHAMBERS, PETER
<u>08792712</u>	<u>5825199</u>	250	01/30/1997	REPROGRAMMABLE STATE MACHINE AND METHOD THEREFOR	CHAMBERS, PETER
<u>08792713</u>	<u>5796994</u>	250	01/30/1997	PATCH MECHANISM FOR ALLOWING DYNAMIC MODIFICATIONS OF THE BEHAVIOR OF A STATE MACHINE	CHAMBERS, PETER
<u>08838021</u>	<u>5961640</u>	150	04/22/1997	VIRTUAL CONTIGUOUS FIFO HAVING THE PROVISION OF PACKET-DRIVEN AUTOMATIC ENDIAN CONVERSION	CHAMBERS, PETER
<u>08846294</u>	<u>6016315</u>	150	04/30/1997	VIRTUAL CONTIGUOUS FIFO FOR COMBINING MULTIPLE DATA PACKETS INTO A SINGLE CONTIGUOUS STREAM	CHAMBERS, PETER
<u>08873099</u>	<u>6108738</u>	150	06/10/1997	MULTI-MASTER PCI BUS SYSTEM WITHIN A SINGLE INTEGRATED CIRCUIT	CHAMBERS, PETER

<u>08878866</u>	<u>5999171</u>	150	06/19/1997	DETECTION OF OBJECTS ON A COMPUTER DISPLAY	CHAMBERS, PETER
<u>08879152</u>	<u>5995112</u>	150	06/19/1997	COLOR SIGNATURE DETECTION OF OBJECTS ON A COMPUTER DISPLAY	CHAMBERS, PETER
<u>08897216</u>	<u>5884052</u>	150	07/14/1997	SMART RETRY MECHANISM TO PROGRAM THE RETRY LATENCY OF A PCI INITIATOR AGENT	CHAMBERS, PETER
<u>08901465</u>	<u>6012115</u>	150	07/28/1997	METHOD AND SYSTEM FOR ACCURATE TEMPORAL DETERMINATION OF REAL-TIME EVENTS WITHIN A UNIVERSAL SERIAL BUS SYSTEM	CHAMBERS, PETER
<u>08904918</u>	<u>5949251</u>	150	08/01/1997	REGISTER-BASED PROGRAMMABLE POST-SILICON SYSTEM TO PATCH AND DYNAMICALLY MODIFY THE BEHAVIOR OF SYNCHRONOUS STATE MACHINES	CHAMBERS, PETER
<u>08960483</u>	<u>5958020</u>	150	10/29/1997	REAL TIME EVENT DETERMINATION IN A UNIVERSAL SERIAL BUS SYSTEM	CHAMBERS, PETER
<u>09010217</u>	<u>6040788</u>	150	01/21/1998	CACHE BASED SCAN MATRIX KEYBOARD CONTROLLER	CHAMBERS, PETER
<u>09020629</u>	<u>6445383</u>	150	02/09/1998	SYSTEM TO DETECT A POWER MANAGEMENT SYSTEM RESUME EVENT FROM A STYLUS AND TOUCH SCREEN	CHAMBERS, PETER
<u>09082618</u>	Not Issued	161	05/19/1998	METHOD AND SYSTEM FOR REAL TIME PCI-BASED HARDWARE ACCELERATION OF SYSTEM DEVELOPMENT AND HDL SIMULATIONS	CHAMBERS, PETER
<u>09177789</u>	<u>6324663</u>	150	10/22/1998	SYSTEM AND METHOD TO TEST INTERNAL PCI AGENTS	CHAMBERS, PETER
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<u>09210103</u>	<u>6178478</u>	150	12/11/1998	SMART TARGET MECHANISM FOR ELIMINATING DUAL ADDRESS CYCLES IN A PERIPHERAL COMPONENT INTERCONNECT ENVIRONMENT	CHAMBERS, PETER
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<u>09239500</u>	<u>6301631</u>	250	01/28/1999	MEMORY MAPPING METHOD FOR ELIMINATING DUAL ADDRESS CYCLES IN A PERIPHERAL COMPONENT INTERCONNECT ENVIRONMENT	CHAMBERS, PETER
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<u>09400738</u>	<u>6226701</u>	150	09/21/1999	METHOD AND SYSTEM FOR ACCURATE TEMPORAL DETERMINATION OF REAL-TIME EVENTS WITHIN A UNIVERSAL SERIAL BUS SYSTEM	CHAMBERS, PETER
<u>09535989</u>	<u>6519560</u>	150	03/27/2000	METHOD FOR REDUCING TRANSMISSION BIT RATE IN A TELECOMMUNICATION SYSTEM	CHAMBERS, PETER
<u>09562036</u>	Not Issued	161	05/01/2000	Delay lock loops	CHAMBERS, PETER
<u>09944876</u>	<u>6643811</u>	150	08/31/2001	SYSTEM AND METHOD TO TEST INTERNAL PCI AGENTS	CHAMBERS, PETER
<u>10294469</u>	<u>7166826</u>	150	11/13/2002	AUTOMATIC CONTROL OF LASER DIODE CURRENT AND OPTICAL POWER OUTPUT	CHAMBERS, PETER
<u>10336296</u>	<u>6898680</u>	150	01/03/2003	MINIMIZATION OF OVERHEAD OF NON-VOLATILE MEMORY OPERATION	CHAMBERS, PETER
<u>10340014</u>	<u>6810347</u>	150	01/09/2003	ROBUST POWER-ON METER AND METHOD	CHAMBERS, PETER
<u>10340439</u>	<u>6785191</u>	150	01/09/2003	ROBUST POWER-ON METER AND METHOD USING A LIMITED-WRITE MEMORY	CHAMBERS, PETER
<u>10340443</u>	<u>7013355</u>	150	01/09/2003	DEVICE AND METHOD FOR IMPROVED SERIAL BUS TRANSACTION USING INCREMENTAL ADDRESS DECODE	CHAMBERS, PETER
<u>10362830</u>	Not Issued	41	08/11/2003	COMMUNICATION SYSTEM FOR MONITORING OF PILOT CHANNEL POWER	CHAMBERS, PETER
<u>10471998</u>	Not Issued	83	04/23/2004	Link power convergence system	CHAMBERS, PETER
<u>10759786</u>	Not Issued	30	01/15/2004	Numerical value conversion using a look-up table for coefficient storage	CHAMBERS, PETER
<u>10759987</u>	Not Issued	93	01/15/2004	LASER TURN-ON ACCELERATOR INDEPENDENT OF BIAS CONTROL LOOP BANDWIDTH	CHAMBERS, PETER
<u>10759988</u>	Not Issued	30	01/15/2004	Numerical value conversion using a saturation limited arithmetic logic unit	CHAMBERS, PETER

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09081309	6054823	150	05/19/1998	VERIFICATION OF FAN OPERATION	JUDKINS, III, JOSEPH JAMES
09947043	6555050	150	09/05/2001	DROSS PROCESSING SYSTEM	JUDKINS, JOSEPH A.
60230959	Not Issued	159	09/07/2000	Dross processing system	JUDKINS, JOSEPH A.
10759987	Not Issued	93	01/15/2004	LASER TURN-ON ACCELERATOR INDEPENDENT OF BIAS CONTROL LOOP BANDWIDTH	JUDKINS, JOSEPH J.
11559255	Not Issued	20	11/13/2006	Laser Turn-On Accelerator Independent of Bias Control Loop Bandwidth	JUDKINS, JOSEPH J.
60530022	Not Issued	159	12/15/2003	Numerical value conversion using a saturation limited arithmetic logic unit supporting variable resolution operands	JUDKINS, JOSEPH J.
60530040	Not Issued	159	12/15/2003	Laser turn-on accelerator independent of bias control loop bandwidth	JUDKINS, JOSEPH J.
60530057	Not Issued	159	12/15/2003	Numerical value conversion using a look-up table for coefficient storage	JUDKINS, JOSEPH J.
08889109	6122284	150	07/07/1997	MULTIDROP ANALOG SIGNAL BUS	JUDKINS, JOSEPH J.
09063072	6037732	150	04/21/1998	INTELLIGENT POWER MANAGEMENT FOR A VARIABLE SPEED FAN	JUDKINS, JOSEPH J.
10294469	7166826	150	11/13/2002	AUTOMATIC CONTROL OF LASER DIODE CURRENT AND OPTICAL POWER OUTPUT	JUDKINS, JOSEPH JAMES
10759786	Not Issued	30	01/15/2004	Numerical value conversion using a look-up table for coefficient storage	JUDKINS, JOSEPH JAMES
10759988	Not Issued	30	01/15/2004	Numerical value conversion using a saturation limited arithmetic logic unit supporting variable resolution operands	JUDKINS, JOSEPH JAMES
09256841	6351601	150	02/24/1999	FAN SPEED CONTROL SYSTEM HAVING AN INTEGRATED CIRCUIT FAN CONTROLLER AND A METHOD OF USING THE SAME	JUDKINS, JOSEPH JAMES
08749864	6040668	150	11/14/1996	MONOLITHIC FAN CONTROLLER	JUDKINS,, JOSEPH J.

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